

FIG. 1A

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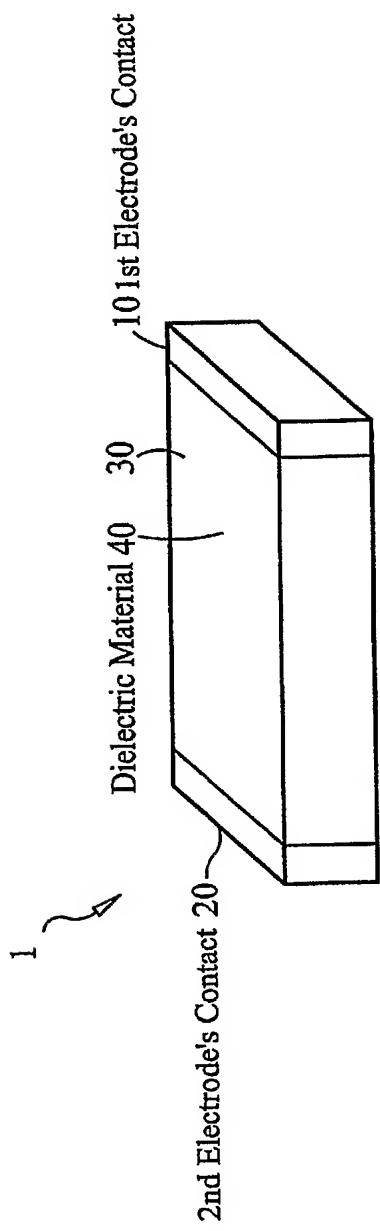


FIG. 1B

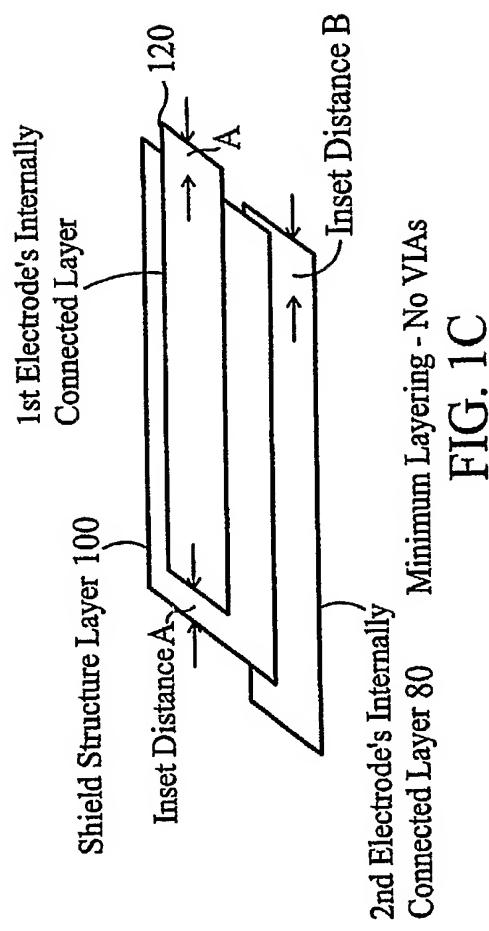


FIG. 1C

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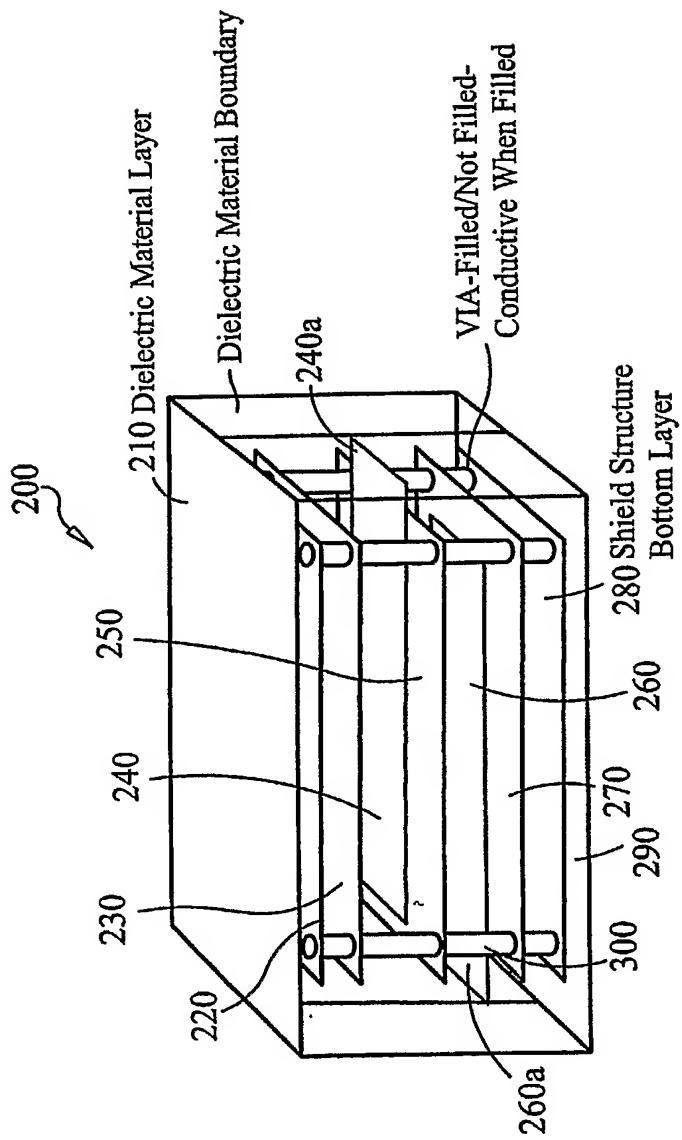


FIG. 2A

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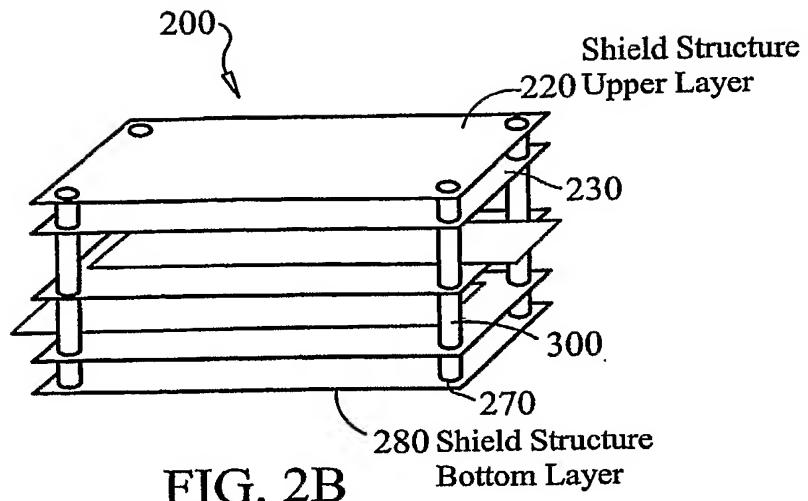


FIG. 2B

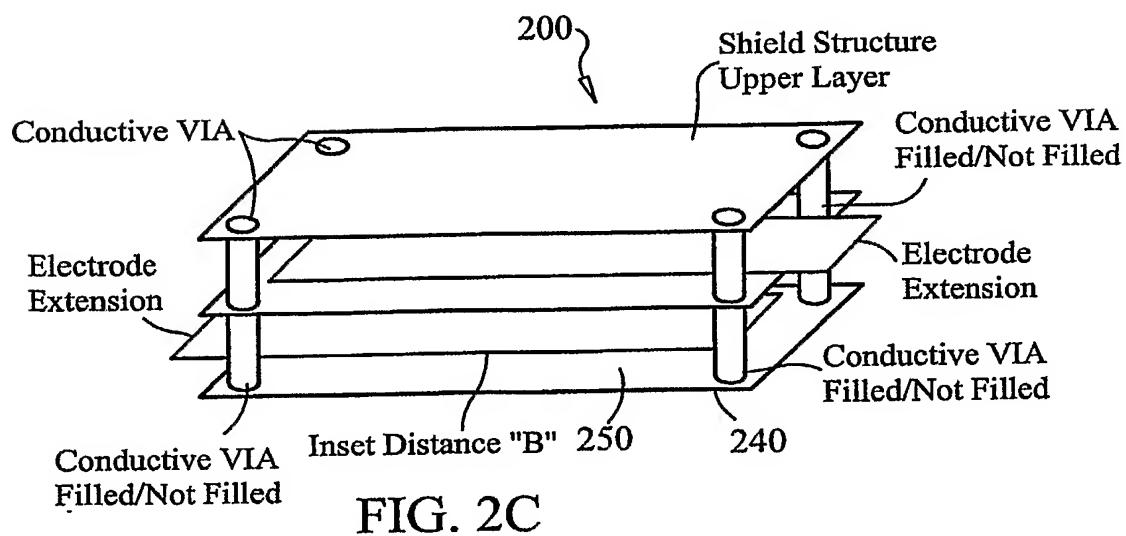


FIG. 2C

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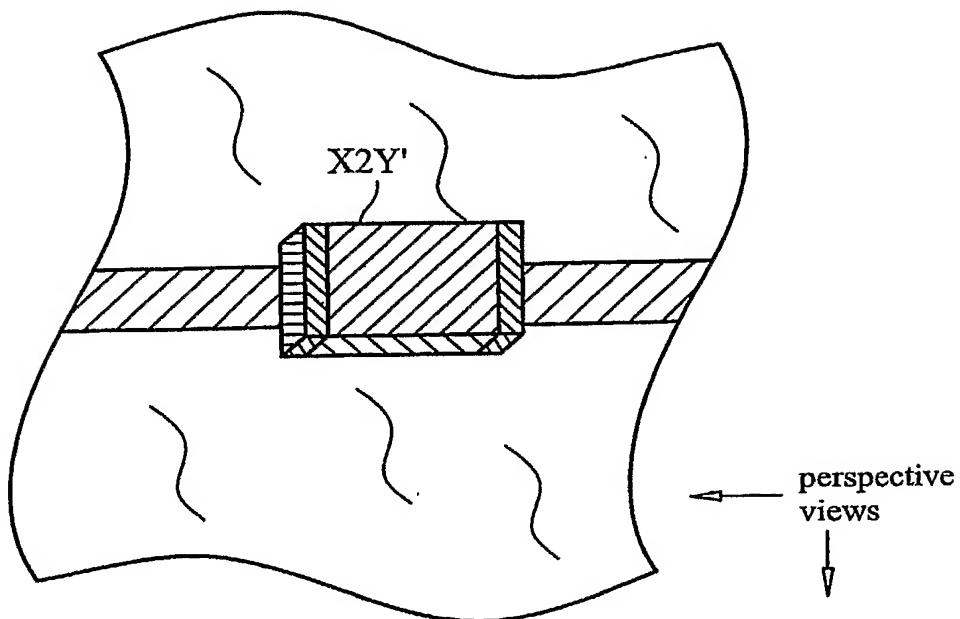


FIG. 3A

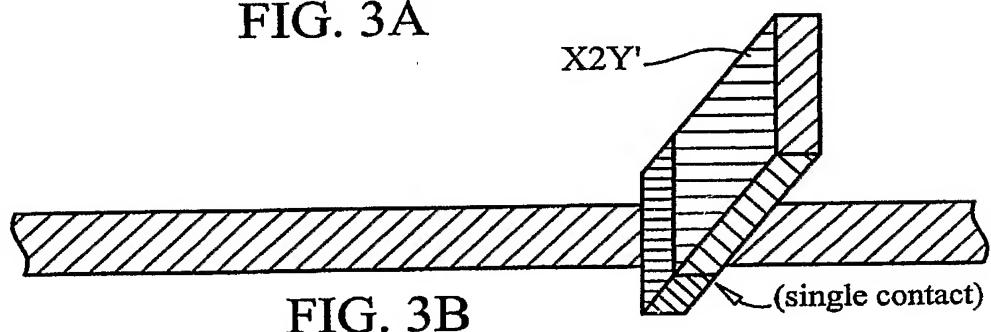


FIG. 3B

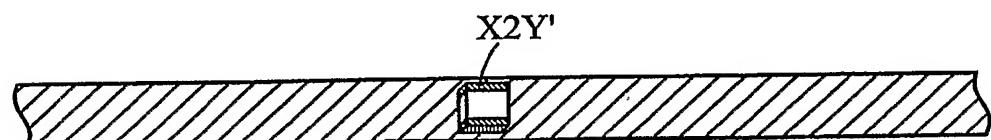


FIG. 3C

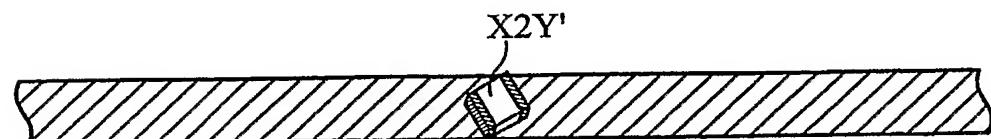
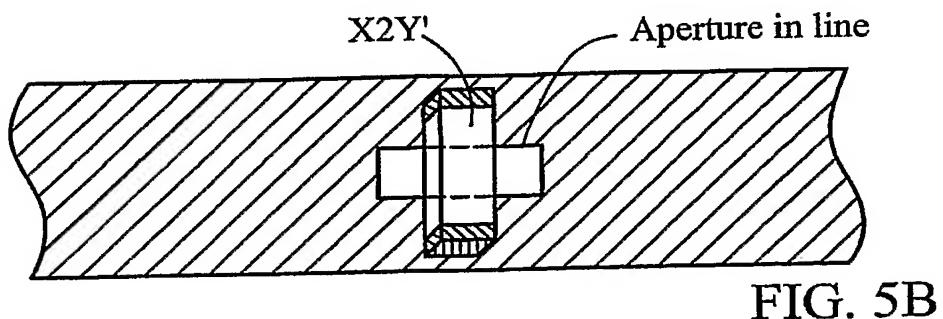
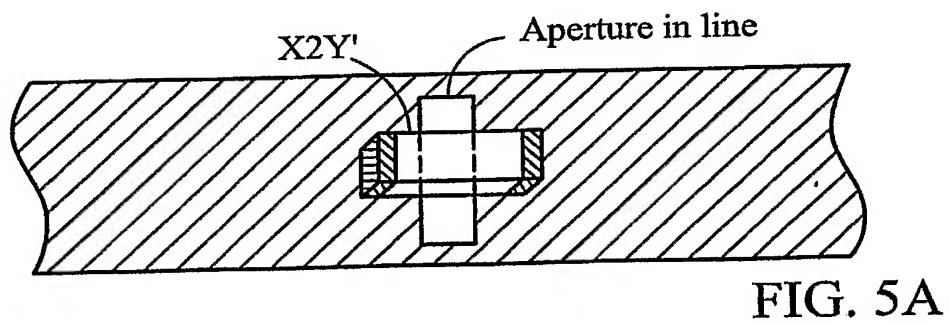
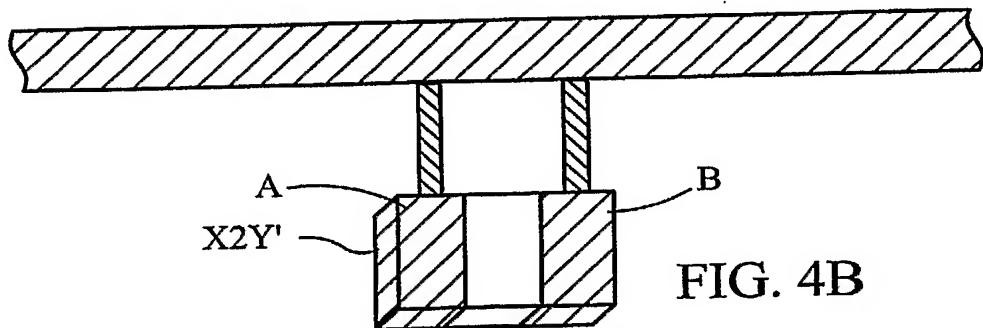
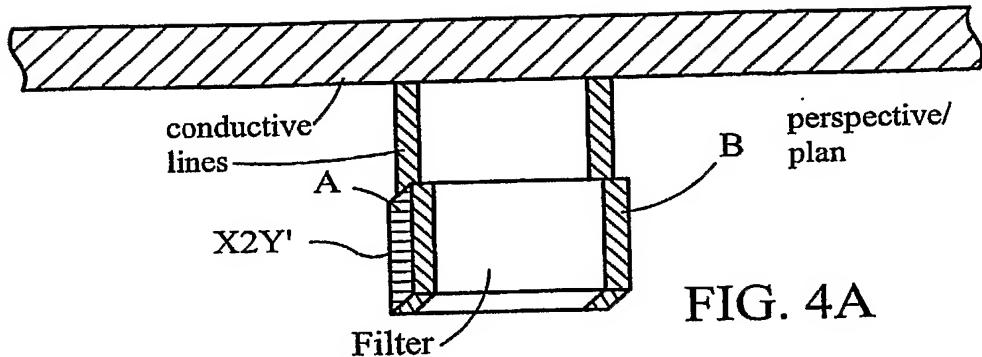


FIG. 3D

SUBSTITUTE SHEET (RULE 26)

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Filter Arrangement

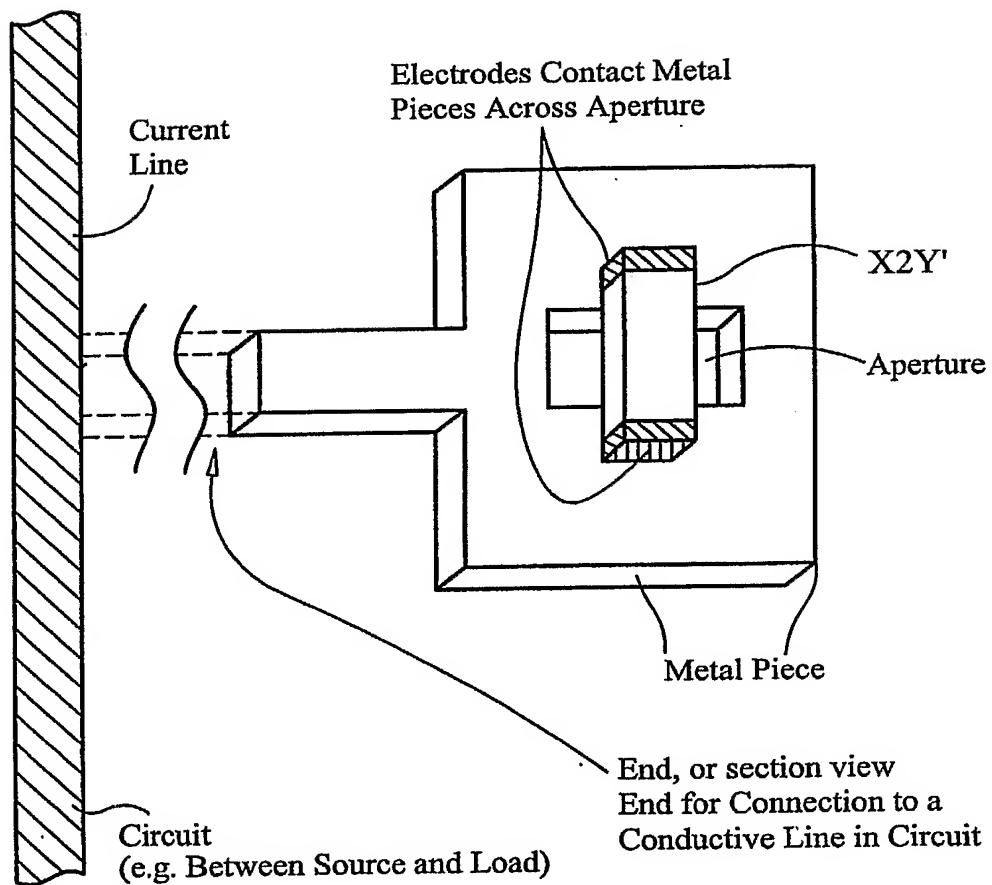
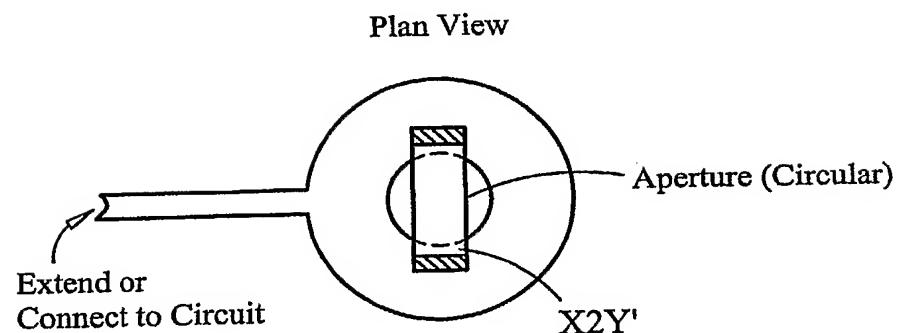
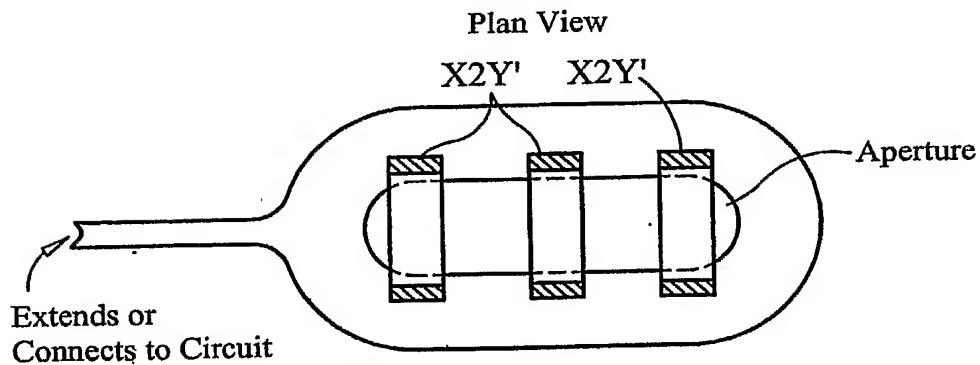


FIG. 6

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Alternative Filter Arrangement**FIG. 7****FIG. 8**

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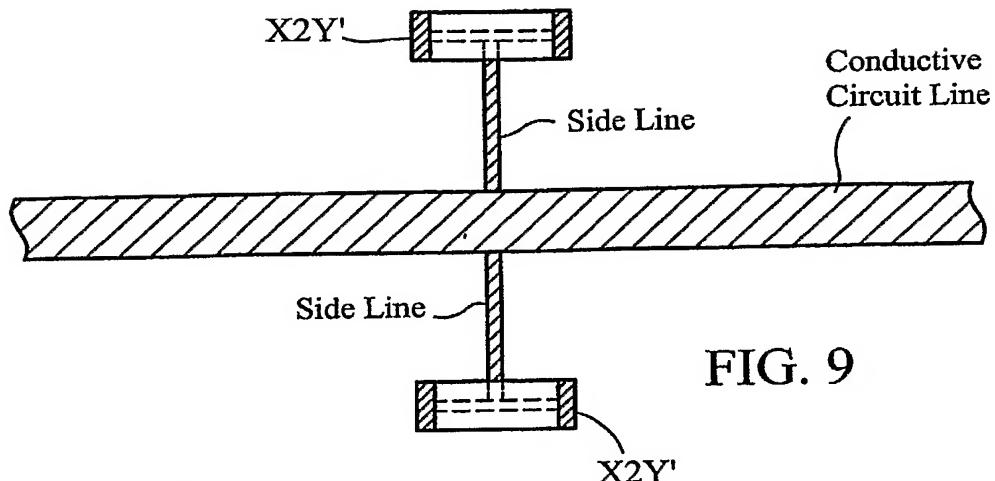


FIG. 9

Plan View

PC or IC
Various X2Y' Arrangements

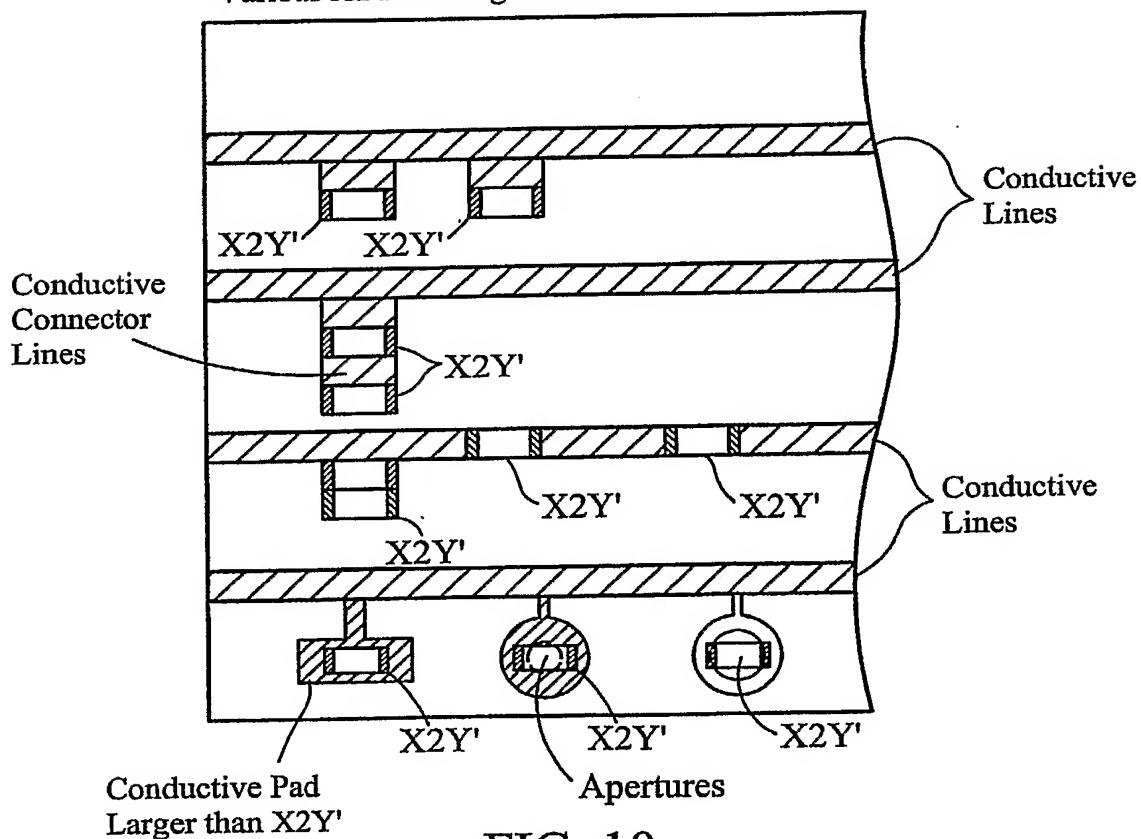


FIG. 10

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Plan View, Partial Section

PC board or CPU with multiple lines or waveguides
for "high frequency" operation.

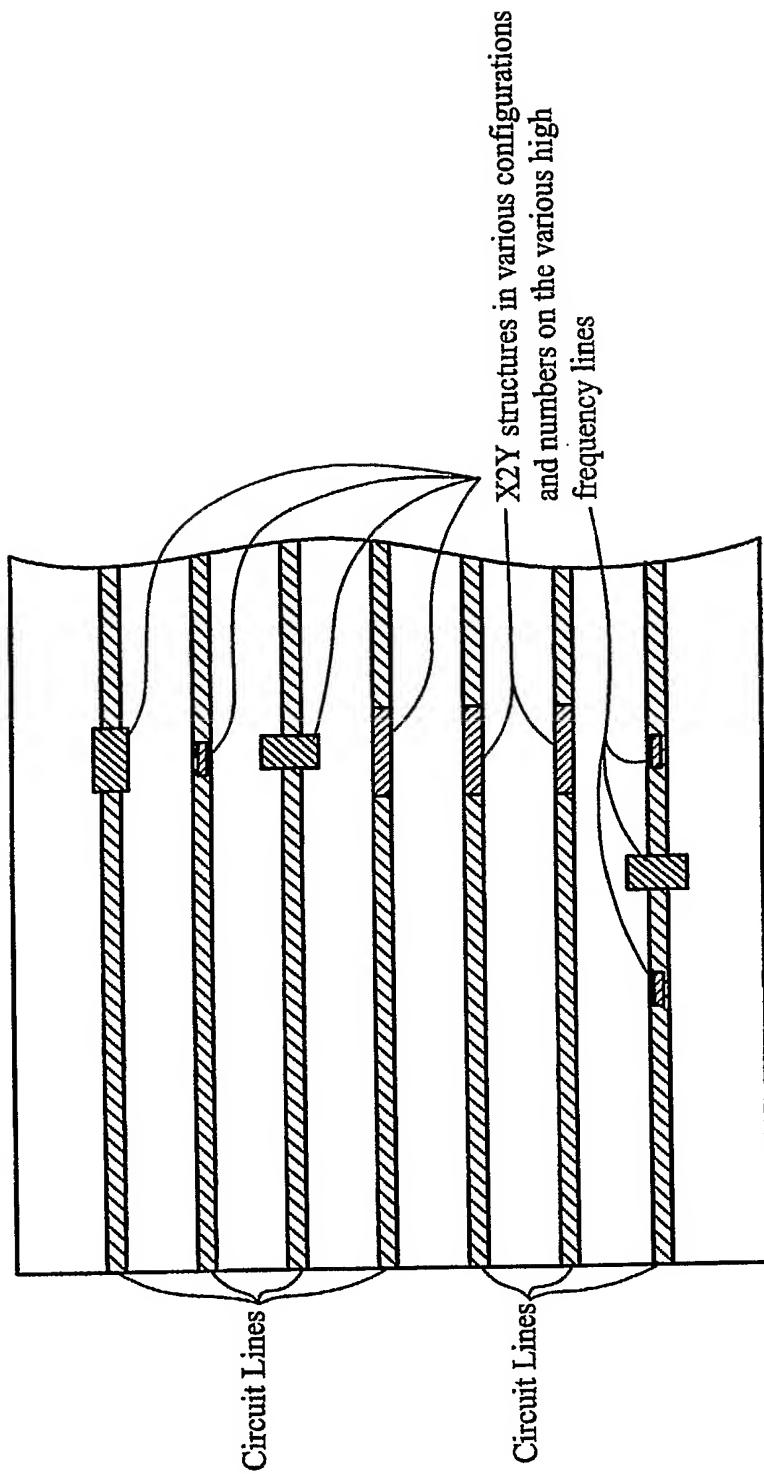
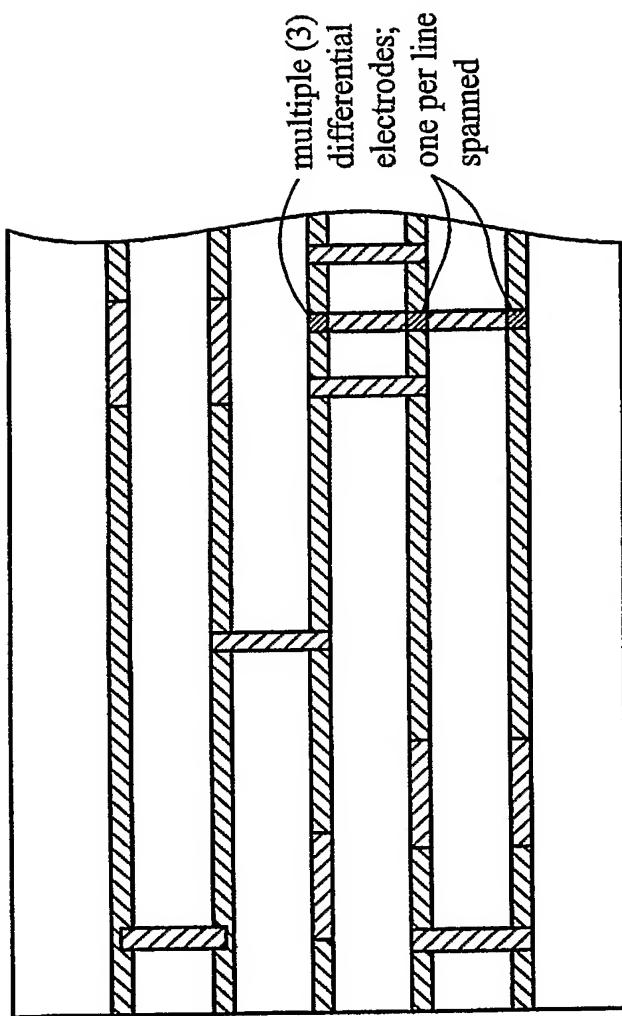


FIG. 11

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Plan View, Partial Section

PC board or CPU with multiple lines or waveguides
for "high frequency" operation.



X2Y' structure in various configurations
and number; some spanning at least 2 lines.
Preferably, one differential electrode per
line spanned.

FIG. 12

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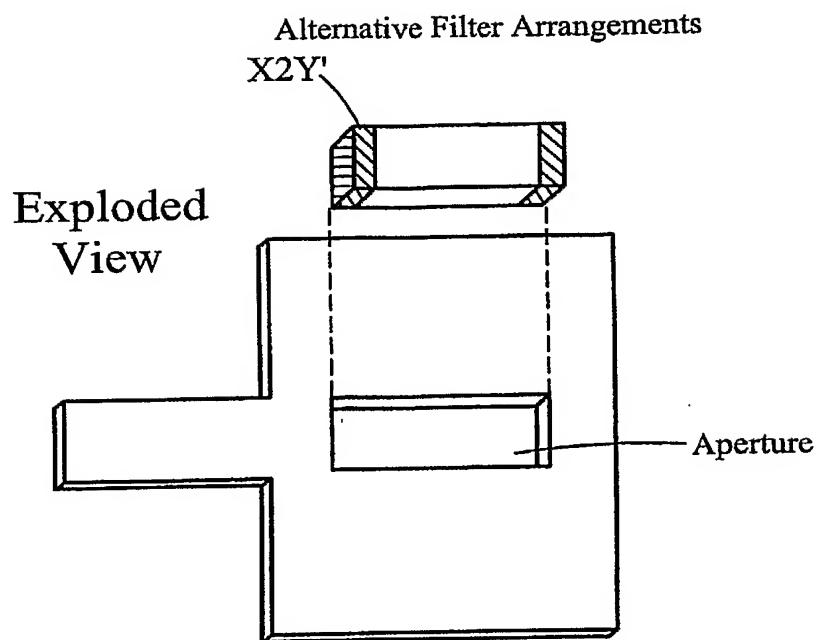


FIG. 13A

Side View

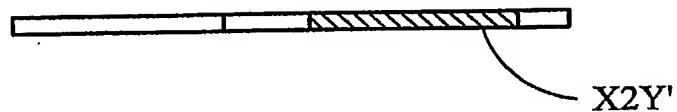


FIG. 13B

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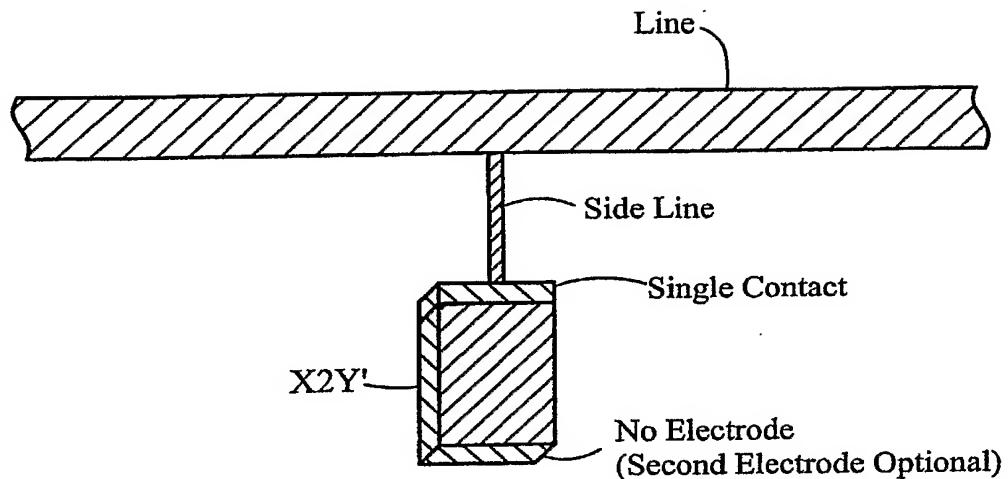


FIG. 14

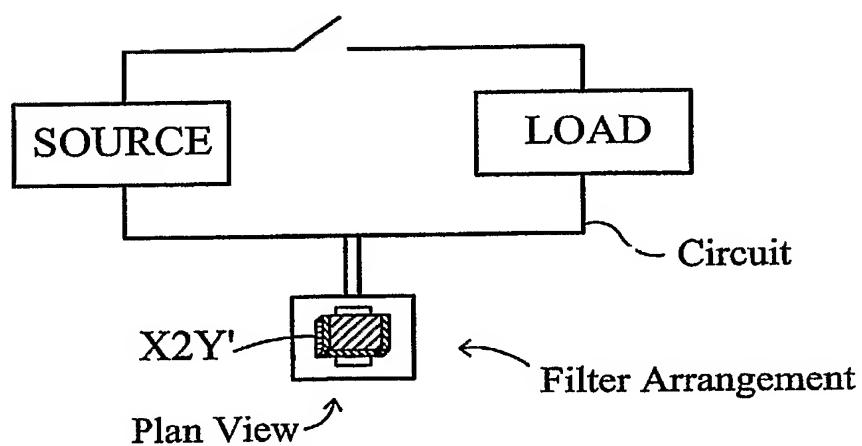


FIG. 15

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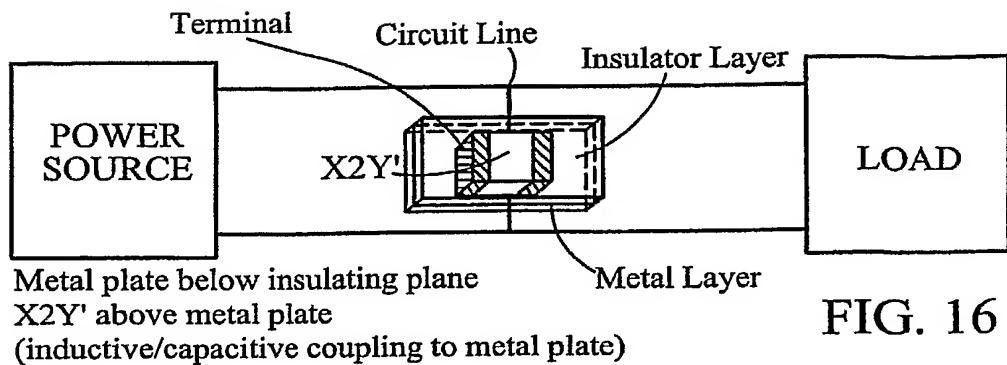
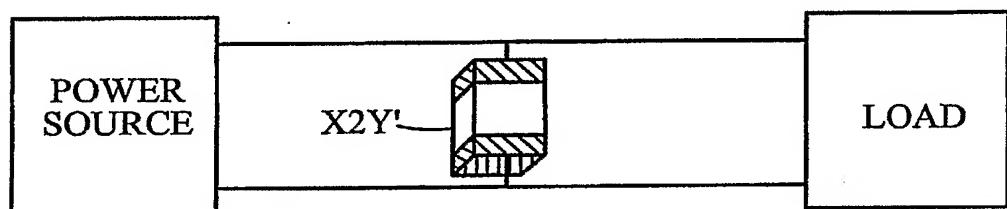


FIG. 16



Circuit with X2Y' (X2Y having no ground or shielding structure electrode)

FIG. 17

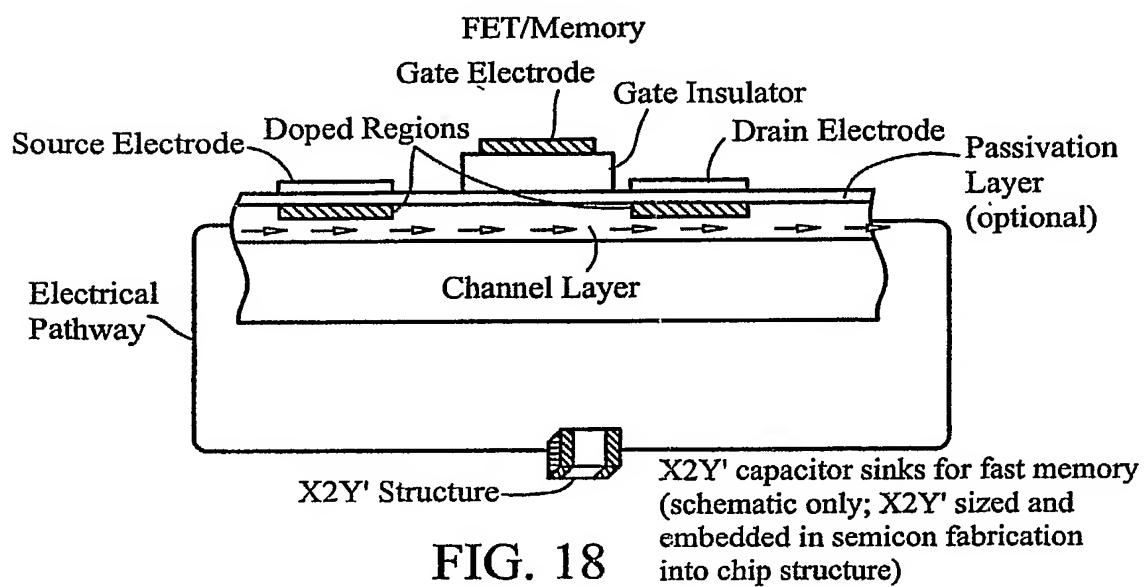


FIG. 18

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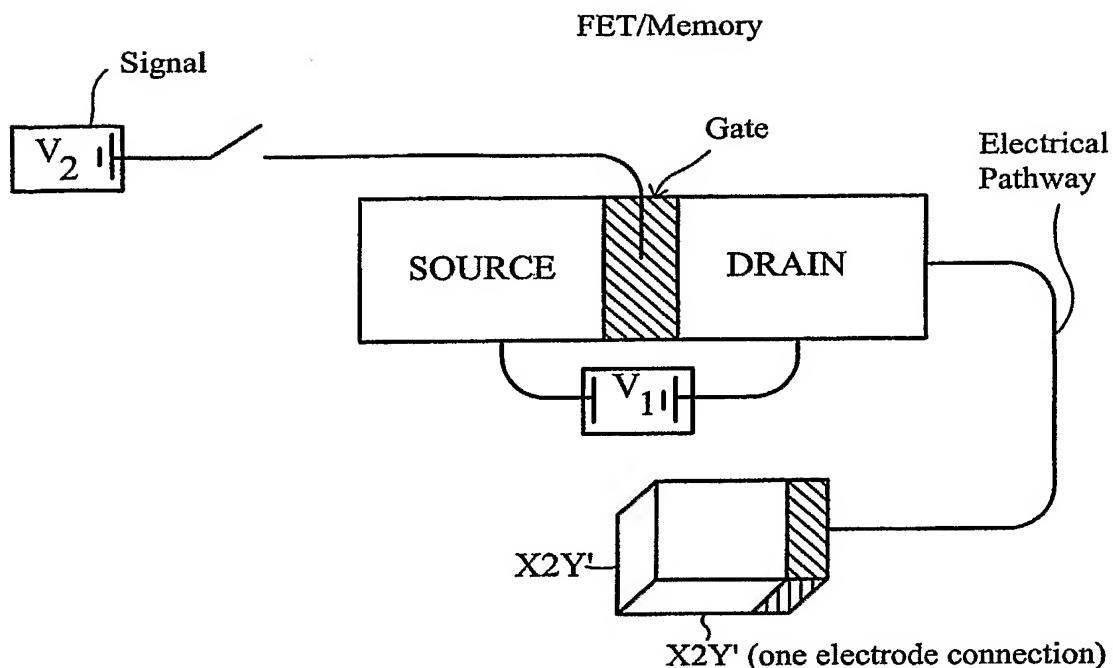


FIG. 19A

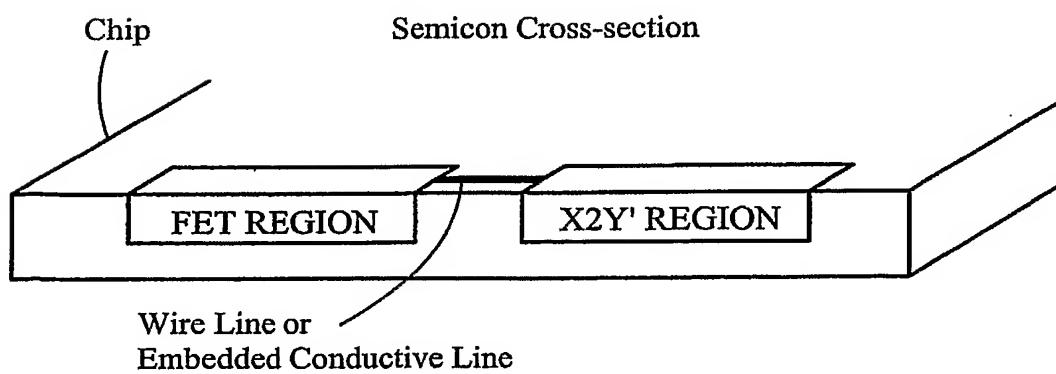


FIG. 19B

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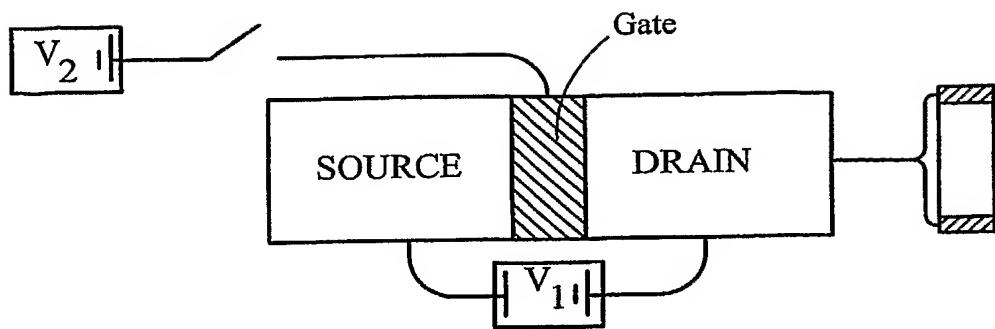


FIG. 20A

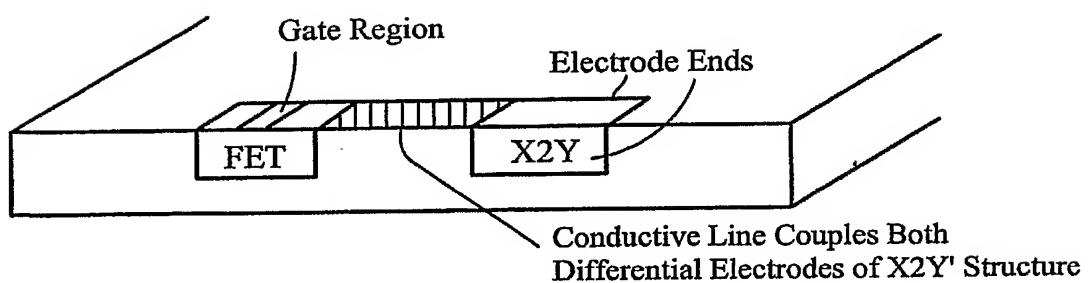


FIG. 20B

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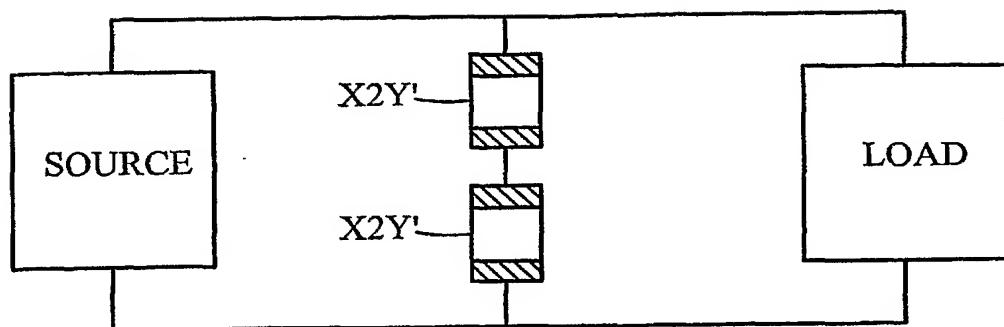


FIG. 21

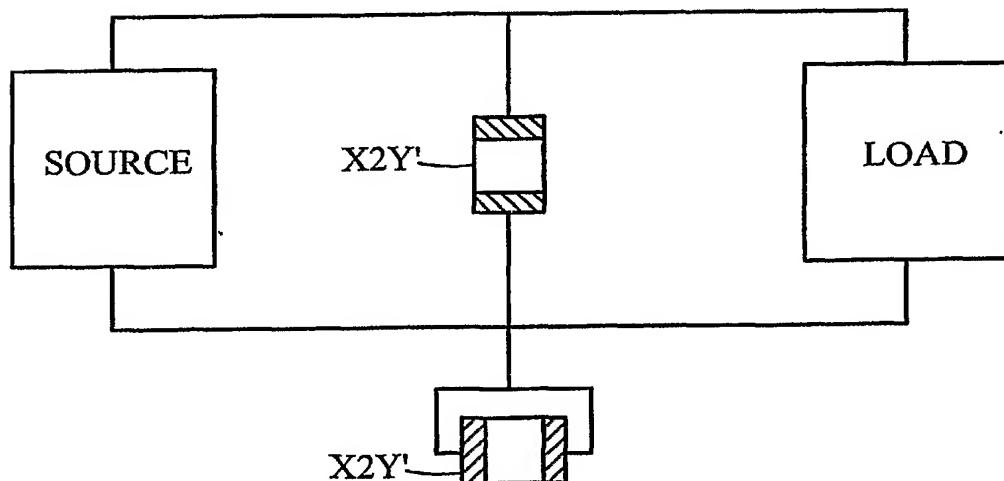


FIG. 22

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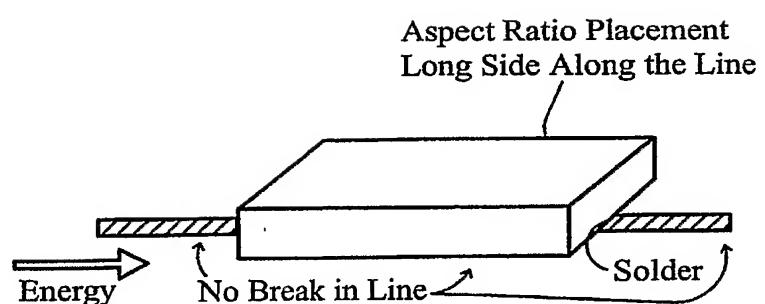


FIG. 23A

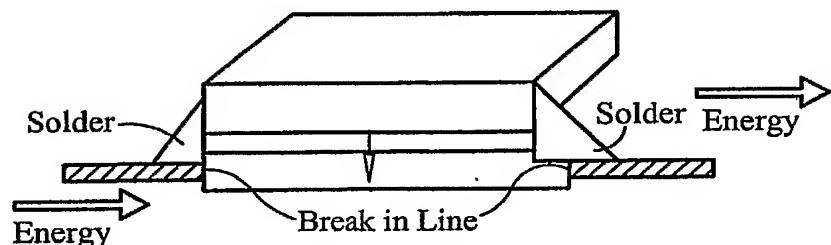


FIG. 23B

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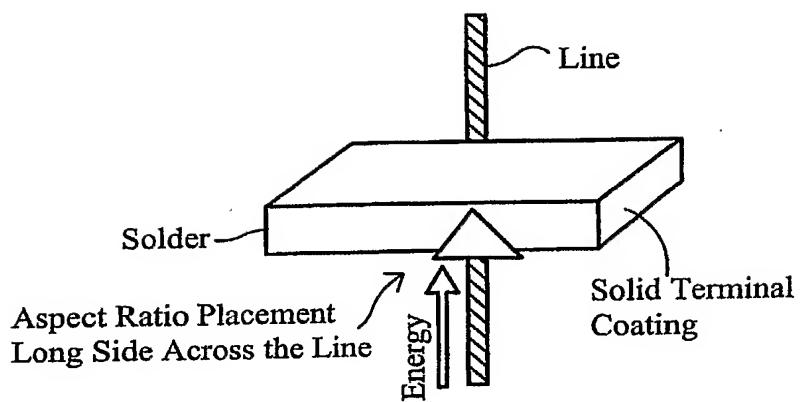


FIG. 23C

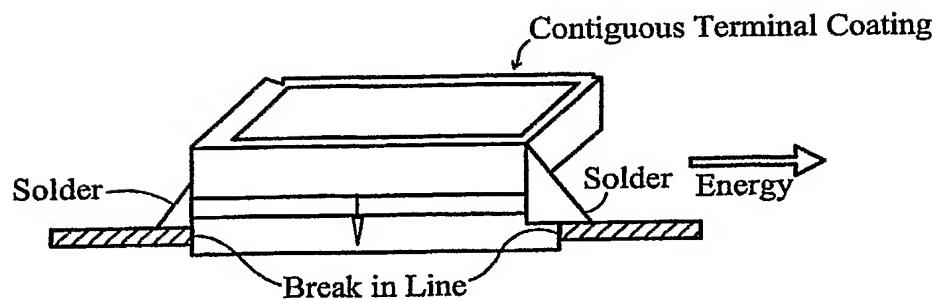


FIG. 24

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Side View

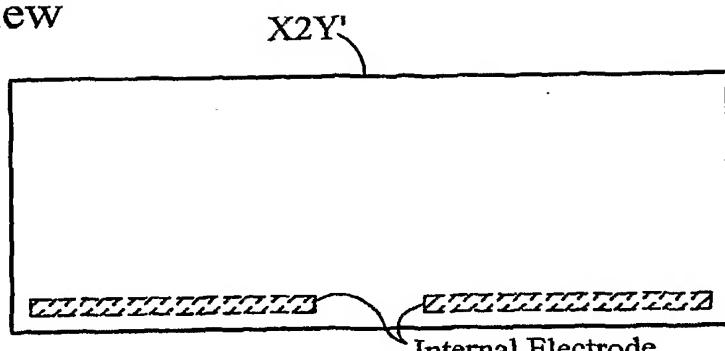


FIG. 25A

Internal Electrode Pad Locations

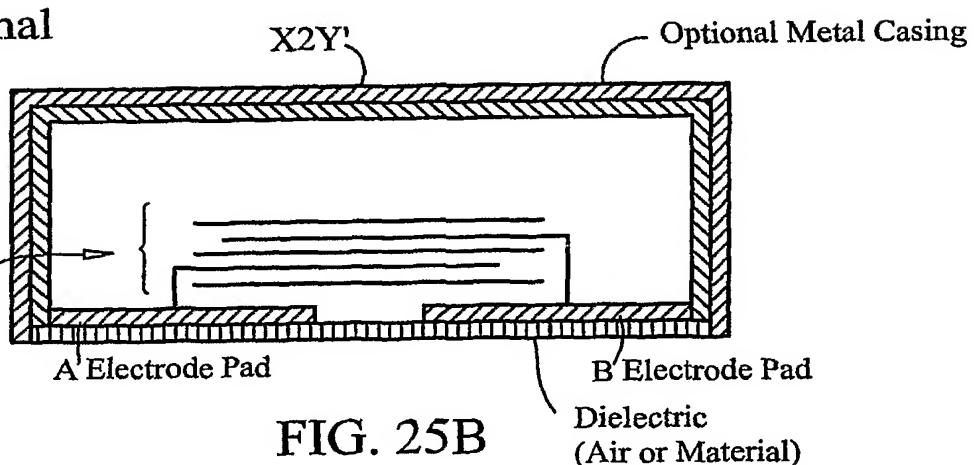
Side
Sectional
View

FIG. 25B

(X2Y 5 Layer Stack)
SHIELD LAYER
B ELECTRODE LAYER
SHIELD LAYER
A ELECTRODE LAYER
SHIELD LAYER

FIG. 25C

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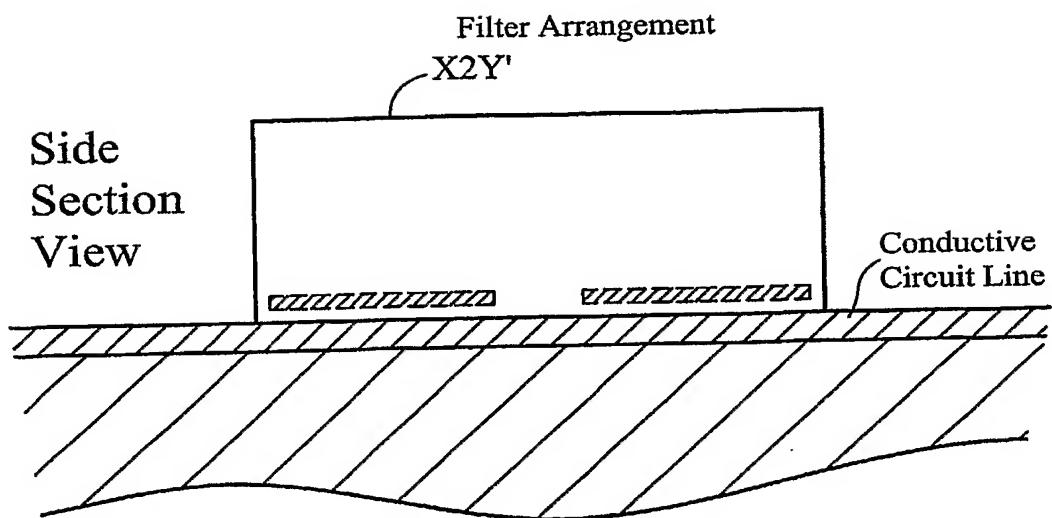


FIG. 26A

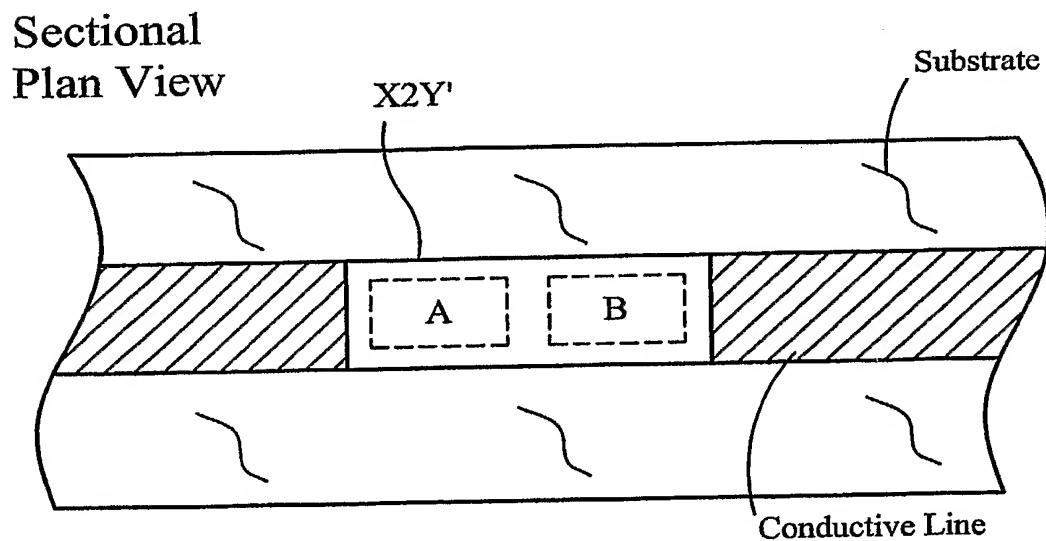


FIG. 26B

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Schematic View in Plan View

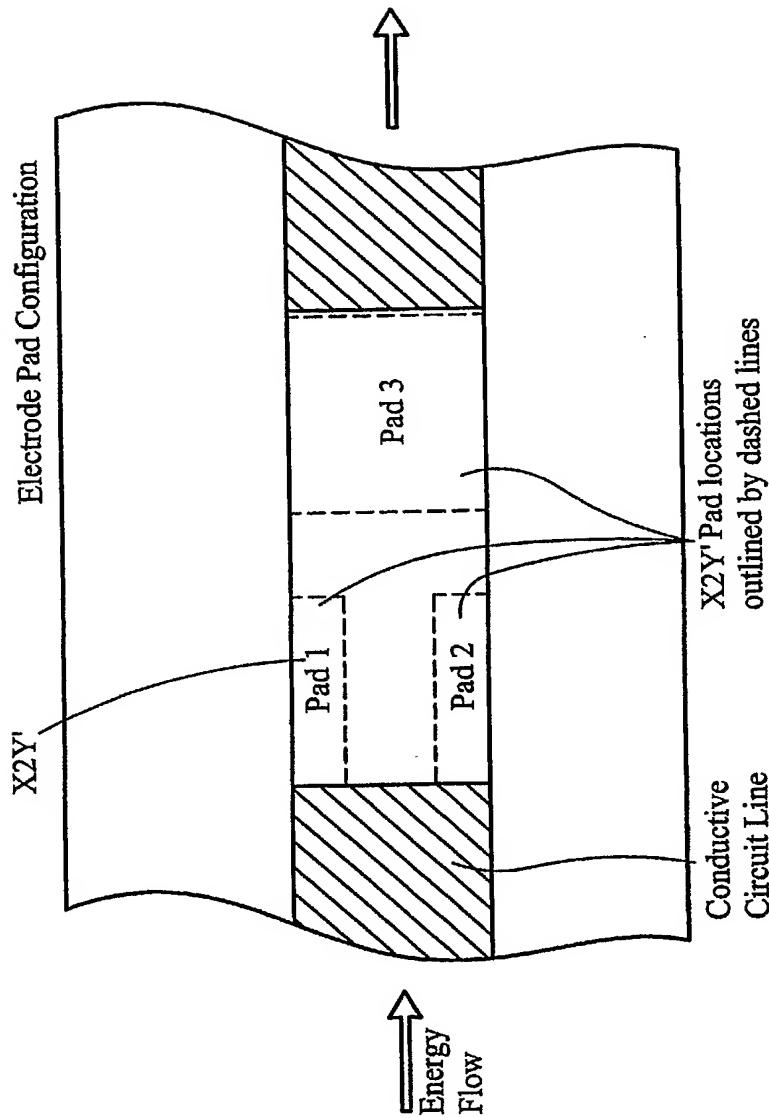


FIG. 27